WHAT IS CLAIMED IS:

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1. An electronic control system receiving a video signal from a video signal source for visual presentation on a flat panel display, which comprises:

a universal video input selector means for determining the format of a plurality of video sources that can automatically extract synchronization components and image components from said video signal;

color reduction means in electrical communication with said universal video input selector means for reducing said image components from primary color signals when driving a flat panel display into a display image;

storage means in electrical communication with said color reduction means for storing said display image; and

timing control means in electrical communication with said universal video input selector means, said color reduction means, and said storage means for controlling the processing of said video signal at the incoming video rate, and controlling a reading of said storage means for outputting said display image to said flat panel display.

2. An electronic control system receiving a video signal from a video signal source for visual presentation on a flat panel display, which comprises:

video input connector means for receiving composite and component video signals, and for generating a first code indicating types of said video signals;

composite video converter means in electrical communication with said video input connector means for separating color components and luminance components from said video signals;

video input selector means in electrical communication with said video input connector means and said composite video converter means for selecting between said color components and said video signals;

synchronization signal means in electrical communication with said video input connection means, said composite video converter means and said video input selector means for extracting horizontal synchronization signals and vertical synchronization signals from said video signals;

A/D converter means in electrical communication with said video input selector means for receiving said color components and said luminance components from said video input selector means to produce digital color signals;

Color to monochrome reduction means in electrical communication with said A/D converter means and receiving said digital color signals for mixing said digital color signals in accordance with weighting formulas to provide monochrome-to-monochrome, monochrome-to-color, color-to-monochrome, and color-to-color transition signals;

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frame buffer means in electrical communication with said color-to-monochrome reduction means and said A/D converter means for storing said digital color signals and said transition signals at a first data rate and asynchronously outputting said digital signals and said transition signals at a second data rate compatible with said flat panel display;

microprocessor means in electrical communication with said video input connector means, said composite video converter means, said video input selector means, said synchronization signal separation means, said A/D converter means, and said color-to-monochrome reduction means, and receiving said first code and a second code, for determining video formats of said video signals and flat panel display types, and for controlling the operation of said electronic control means, and for supplying said weighting formulas to said color-to-monochrome reduction means;

pixel clock generator means in electrical communication with said microprocessor means, said synchronization signal separation means, and said A/D converter means, and responsive to said horizontal synchronization signals, said vertical synchronization signals, and said microprocessor means for generating pixel clock signals which are synchronized to said horizontal synchronization signals and supplied to said A/D converter means to control the processing of said video signals;

frame buffer input control means in electrical communication with said synchronization signal separation means, said frame buffer means, said pixel clock generator means, and said microprocessor means for controlling the storage of said digital color signals and said transition signals into said frame buffer means;

flat panel timing generator means in electrical communication with said microprocessor means, said microprocessor means, said pixel clock generator means, and said synchronization signal separation means for generating output control timing signals to drive said flat panel display, fit an image on said flat panel display, and control power sequencing in turning said electronic control system on and off as said video signals are received and interrupted;

image size/position control means in electrical communication with said microprocessor means and said flat panel timing generator means for generating image control signals to control size, position and orientation of a video image presented on said flat panel display;

frame buffer output control means in electrical communication with said microprocessor means, said frame buffer means, and said image size/position control means for controlling addressing and output data rate of said digital color signals and said transition signals stored in said frame buffer means;

power circuit means in electrical communication with said microprocessor means for supplying power-up voltages to said electronic control system; and

flat panel interface module means in electrical communication with said microprocessor means, said flat panel timing generator means, said power circuit means, and said frame buffer means, and receiving said digital color signals and said transition signals from said frame buffer means at said second data rate, said output control timing signals from said flat panel timing generator means, and a power-up voltage from said power circuit means, for routing said digital

color signals, said transition signals, said output control timing signals, and said power-up voltage to said flat panel display system, and for supplying said second code to said microprocessor means to identify a flat panel display type.

3. The electronic control system of Claim 2, wherein said synchronization signal separation means includes a synchronization signal detector for locking onto said horizontal synchronization signals and said vertical synchronization signals.

4. The electronic control system of Claim 2, wherein said video input connector means is a plug-in module which may be interchanged with selected ones of plural other plug-in modules to accommodate any type and format of said video signals.

5. The electronic control system of Claim 2, wherein said primary color components are red, green and blue color signals.

6. The electronic control system of Claim 2, wherein said video input connector means includes a selectably variable voltage reference to accommodate a wide range of amplitudes of said video signals.

7. The electronics control system of Claim 2, wherein said frame buffer means is comprised of plug-in frame buffer modules of varying bit length and frame size to accommodate a wide variety of video formats.

8. The electronic control system of Claim 2, wherein said electronic control system includes user controls in electrical communication with said microprocessor means for changing said weighting formulas and varying image contrast, position, brightness, and orientation, and shrinking and expanding said image on said flat panel display.

9. The electronic control system of Claim 8, wherein said user controls are comprised of analog controls, digital controls and configuration switches.

10. The electronic control system of Claim 2, wherein said first data rate is an incoming video data rate and said second data rate is at a flat panel display data rate.

11. The electronic control system of Claim 2, wherein said A/D converter means is comprised of a pair of A/D converters per video color signal, wherein one of said pair of A/D converters digitizes even pixels and another of said pair of A/D converters digitizes odd pixels for accommodating high data rates.

12. The electronic control system of Claim 2, wherein said video types include VGA with said vertical synchronization signals and said horizontal synchronization signals separated, RS-170/RS-343 sync-on green, RS-170/RS-343 RGB separate composite sync, composite NTSC and PAL types, and said video formats include NTSC, PAL, HDTV, SECAM, XGA, SVGA, RGB, VGA 640 X 480 Graphics, VGA 80 X 25 Text, and VGA 640 X 350 Graphics.

13. The electronic control system of Claim 2, wherein said microprocessor means determines said video formats on basis of number of said horizontal synchronization signals that are detected by said synchronization signal separation means for each of said vertical

synchronization signals detected by said synchronization signal separation means, and polarity of said vertical synchronization signals and said horizontal synchronization signals.

14. The electronic control system of Claim 2, wherein said electronic control system accommodates video resolutions up to at least 2048 X 2048 rows and columns.

15. The electronic control system of Claim 2, wherein said video input connector means may be any one of a 15 pin VGA, BNC, or RCA type connectors.

16. The electronic control system of Claim 2, wherein said flat panel interface module means is a plug-in mode which may be interchanged with selected one of plural other plug-in modules to accommodate any type of said flat panel display.

17. The electronic control system of Claim 2, wherein said plug-in module may be any one of a color or monochrome LCD, electroluminescent, gas plasma or FED flat panel display.

18. The electronic control system of Claim 2 wherein said second code may identify any one of at least 256 different flat panel display types.

19. The electronic control system of Claim 2, wherein said video signals may be any one of interlaced and non-interlaced video signals.

20. A system for controlling the size, position and orientation of a video image presented on a flat panel display, and in electrical communication with a memory system having stored therein a video image for display on said flat panel display, and receiving a video signal from a video source, which comprises:

timing control means receiving said video signal from said video source at said video signal data rate for generating therefrom enable, vertical synchronization, horizontal synchronization, and first clock signals for driving said flat panel display, generating column start, row start, column replicate, and row replicate control signals for sizing said video image while maintaining said video signal resolution, and generating first control signals for reading said video image information in said memory system;

image size/position control means in electrical communication with said timing control means and responsive to said column start, row start, column replicate, and row replicate control signals and said first control signals for generating output column address control signals, and output row address control signals for said memory system; and a pixel clock signal; and

frame buffer output control means in electrical communication with said timing control means, said memory system, said image size/position control means, and said flat panel display, and responsive to said pixel clock signal for reading said video image from said memory system.

21. An analog-to-digital converter system for digitizing a video signal received from a video source at a high data rate, which comprises:

timing control means in electrical communication with said video source and receiving said video signal for generating a pixel clock signal in synchronization with a horizontal synchronization signal of said video signal;

a first analog-to-digital converter in electrical communication with said timing control means and said video source, and receiving said video signal and said pixel clock signal, and generating therefrom odd pixel data signals;

an inverter in electrical communication with said timing control means, and receiving said pixel clock signal, and producing an inverted pixel clock signal;

a second analog-to-digital converter in electrical communication with said inverter and said video source, and receiving said inverted pixel clock signal and said video signal, and generating therefrom an even pixel data signals; and

a two-to-one multiplexer in electrical communication with said first analog-to-digital converter, said timing control means, said inverter, and said second analog-to-digital converter, and interlacing said odd pixel data signals and said even pixel data signals to produce a pixel signal representative of said video signal with no loss of resolution.

22. A system for reducing video color signals received from a video source to monochrome grey scale signals, which comprises:

digitizing means in electrical communication with said video source for digitizing said video color signals to produce a red digital color signal, a green digital color signal, and a blue digital color signal;

an AND gate logic means in electrical communication with said digitizing means and receiving said red digital color signal, said green digital color signal, and said blue digital color signal, for producing first logic signals;

memory means in electrical communication with said AND gate logic means and having stored therein weighting values for mixing said red digital color signal, said green digital color signal and said blue digital color signal;

microprocessor means in electrical communication with said memory means for storing said weighting values; and

OR gate logic means in electrical communication with said AND gate logic means and receiving said first logic signals to produce a monochrome grey scale video signal for presentation on said flat panel display.

23. A method of power-up and power down sequencing in a electronic control system for a flat panel display, said electronic control system having a first timing control system for generating digital synchronization signals, a second timing control system in electrical communication with said first timing control system for generating digital color signals and digital transition signals from a video signal received from a video source, a memory system in electrical communication with said first timing control system, said second timing control system, and said flat panel display, and having stored therein said digital color signals and said digital transition signals, and a backlight inverter power supply, comprising the steps of:

supplying power to said flat panel display system;

T1 seconds after supplying power to said flat panel display, supplying power to said first timing control system;

T2 seconds after supplying power to said flat panel display, supplying power to said second timing control system and said memory system;

T3 seconds after supplying power to said flat panel display, supplying power to said backlight power supply;

When power to said electronic control system is to be turned off, turning off the power to said backlight power supply first;

T4 seconds after power to said backlight power supply is turned off, turning power to said second timing control system and said memory system off;

T5 seconds after power to said backlight power supply is turned off, turning power to said
first timing control system off; and

T6 seconds after power to said backlight power supply is turned off, turning power to said flat panel display off.

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